As shown in Fig. 6 of ***Drowley***, ***Drowley*** does not have a contact hole reaching the drain region (or source region) of the MOS transistor 32. Furthermore, ***Drowley*** does not suggest or recognize the problem of P-N junction leak current flowing via a contact hole in the drain region of the MOS transistor. ***Drowley*** provides a structure which would not have a leak current problem since it does not have a contact hole to flow a leak current. It is believed the amended claims distinguish the present invention from ***Drowley.***

Claims 2, 3, 5 and 6 were rejected under 35 USC §103(a) as being unpatentable over ***Drowley et al.*** in view of ***Park***. Favorable reconsideration of this rejection is requested in view of the amendments made herein.

For the same reasons discussed above, the amended claims distinguish over the cited art. With respect to ***Park***, *Park* fails to provide the teachings which ***Drowley*** lacks. Furthermore, ***Park*** would not have motivated one of ordinary skill in the art to have modified ***Drowley et al.*** which would have rendered the presently claimed invention unpatentable.

Claim 4 was rejected under 35 USC §103(a) as being unpatentable over ***Drowley et al.*** in view of ***Park*** and in further view of ***Islam.*** Favorable reconsideration of this rejection is requested since *Islam* fails to provide the teachings which ***Drowley et al.*** and ***Park*** lack as discussed above.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should be Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone the applicants' undersigned attorney.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: (1) Version with markings to show changes made
(2) Petition for Extension of Time

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/753,616

IN THE SPECIFICATION:

The specification has been amended as follows:

Paragraph bridging pages 9 and 10 (line 27, page 9 through line 9, page 10) has been amended as follows:

Next, as shown in Fig. 4B and Fig. 12B, the entire surface of the resultant structure is coated with a photoresist film 13 so as to cover the silicon nitride film 11, and an opening portion is provided at a portion corresponding to a P channel MOS transistor formation portion after exposure and developing steps. Phosphorus (P) is ion-injected to the semiconductor substrate 10 through the opening portion under conditions of, for example, 180 keV and 1.4 X [1013/cm2] $10^{13}/cm^2$, and an N type impurity region 41 is formed.

Paragraph beginning at page 10, line 21 has been amended as follows:

Subsequently, a well of a photodiode formation portion is formed. Specifically, boron (B) is ion-injected to the whole of a light receiving portion under conditions of, for example, 600 keV and 3 X [1012/cm2] $10^{12}/cm^2$, and a P type impurity layer (well) 43 is formed in the semiconductor substrate 10.

Paragraph bridging pages 10 and 11 (line 27, page 10 through line 8, page 11) has been amended as follows:

Thereafter, as shown in Fig. 5C and Fig. 13B, the photodiode formation portion and the P channel MOS transistor formation portion are covered with a resist film 17, and boron (B) is ion-injected to an N channel MOS transistor formation portion under conditions of, for example, 140

keV and 8 X [1012/cm2] $\underline{10^{12}/cm^2}$, and a P well 44 is formed. At the same time, a channel stopper layer 44a of an N channel MOS transistor. Thereafter, the resist film 17 is removed.

Paragraph bridging pages 11 and 12 (line 26, page 11 through line 4, page 12) has been amended as follows:

Next, as shown in Fig. 6C and Fig. 14A, a WSi (tungsten silicon) film 21 is grown on the amorphous film 19 to a thickness of 150 nm. Then, the phosphorus (P) is ion-injected under conditions of, for example, 40 keV and 8 X [1015/cm2] $\underline{10^{15}/cm^2}$, thus converting the amorphous silicon film 19 to a low resistance substance.

Paragraph beginning at page 12, line 12 has been amended as follows:

Thereafter, as shown in Fig. 7B and Fig. 14C, the amorphous carbon film, the silicon oxide film 22, the WSi film 21, the amorphous silicon film [20] $\underline{19}$ and the silicon oxide film 18 are etched by photolithography, and gate electrodes of the MOS transistors are formed.

Paragraph beginning at page 12, line 17 has been amended as follows:

Next, as shown in Fig. 7C, a resist film 23 having an opening portion is formed in the photodiode formation portion, and then phosphorus (P) is ion-injected to the photodiode formation portion under conditions of, for example, 20 keV and 4 X [1015/cm2] $\underline{10^{15}/cm^2}$, thus forming an N type impurity region 45. Thereafter, the resist film 23 is removed, and a thermal treatment is carried out at a temperature of 1000 °C and for 10 seconds.

Paragraph bridging pages 12 and 13 (line 25, page 12 through line 6, page 13) has been amended as follows:

Subsequently, as shown in Fig. 8A and Fig. 15A , a resist film 25 that covers the P channel MOS transistor formation portion and a photodiode formation portion is formed, and phosphorus (P) is ion-injected to both sides of the gate electrode of the N channel MOS transistor formation portion under conditions of, for example, 20 keV and 4 X [1013/cm2] $\underline{10^{13}/cm^2}$,thus, forming a low concentration N type impurity region 46. Thereafter, the resist film 25 is removed.

Paragraph beginning at page 14, line 4 has been amended as follows:

Subsequently, as shown in Fig. 16B, a resist film 30 that covers a portion other than P channel MOS transistor formation portion is formed, and BF2 is ion-injected to both sides of the gate electrode of the P channel MOS transistor under conditions of, for example, 20 keV and 3 X [1015/cm2] $\underline{10^{15}/cm^2}$, thus forming a high concentration P type impurity region 48. Thereafter, the resist film 30 is removed.

Paragraph bridging pages 14 and 15 (line 12, page 14 through line 3, page 15) has been amended as follows:

Furthermore, as shown in Fig. 9B and Fig. 16C, a resist film 31 that covers the P channel MOS transistor formation portion is formed, and arsenic (As) is ion-injected to both sides of the gate electrode of the N channel MOS transistor under conditions of, for example, 30 keV and [1015/cm2] $\underline{10^{15}/cm^2}$, thus forming a high concentration P type impurity region 49. Thereafter, the resist film 31 is removed. Then, the P type channel impurity region 48 and the N type impurity region 49 are activated by performing a thermal treatment at 1000 °C and for 10 seconds. Thus, an N channel MOS transistor and a P channel MOS transistor having an LDD

structure are completed. Note that though the drain side of the reset transistor T1 (a side connected to the photodiode) is not formed to the LDD structure, it was confirmed by experiments performed by the inventors of this application that any trouble is not brought about practically even if this side is formed to the LDD structure.

Paragraph beginning at page 15, line 18 has been amended as follows:

Next, as shown in Fig. 10B and Fig. 17C, an insulating film 34 is formed on the entire surface of the resultant structure. This insulating film 34 is formed by laminating, for example, SiON having a thickness of 200 nm and, for example, [SiO2] <u>SiO_2</u> having a thickness of 300 nm. Thereafter, the insulating film 34 is coated with an SOG (Spin On Glass) film 35, thus flattening the surface of the resultant structure.

<u>IN THE CLAIMS</u>:

Please amend claims 1 and 2 as follows:

1. (Amended) A CMOS image sensor comprising:

a photodiode having an impurity region <u>having source and drain regions formed respectively</u> [formed] in a semiconductor substrate; and

[a] first and [a] second MOS transistors formed by introducing impurities into said semiconductor substrate, <u>and</u>

[wherein a silicide film is not formed on a surface of an impurity region of said first MOS transistor having said impurity region connected to said impurity region of said photodiode, said first MOS transistor being positioned at least on one side of said photodiode, and a silicide film is formed on a surface of an impurity region of said second MOS transistor]

an insulating film formed on the first and second MOS transistors, the insulating film having contact holes reaching the source regions and drain regions of the first and second MOS transistors,

wherein a silicide film is not formed on a surface of the drain region of the first MOS transistor which connects to the impurity region of the photodiode, but the silicide film is formed on a surface of the source region of the first MOS transistor which is also the drain region of the second MOS transistor and on a surface of the drain region of the second MOS transistor.

2. (Amended) A CMOS image sensor comprising:

a photodiode having an impurity region formed in semiconductor substrate;

a first MOS transistor formed on said semiconductor substrate, the first MOS transistor having an impurity region as a drain connected to said impurity region of said photodiode;

a second MOS transistor formed on said semiconductor substrate, the second MOS transistor having an impurity region as a source connected to a source of said first MOS transistor; [and]

a third MOS transistor formed on said semiconductor substrate, the third MOS transistor having an impurity region as a source connected to a drain of said second MOS transistor,

[wherein a silicide film is not formed on a surface of said drain of said first MOS transistor, and a silicide film is formed on a surface of the source of said first MOS transistor and surfaces of the sources and the drains of said second and third MOS transistors]and

an insulating film formed on the first, second and third MOS transistors, the insulating film having contact holes reaching the sources and drains of the first, second and third MOS transistors,

wherein a silicide film is not formed on a surface of the drain of the first MOS transistor, but the silicide film is formed on each surface of the sources and drains of the first, second and third MOS transistors except for the drain of the first MOS transistor.